Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **COMP “A”**
2. **INPUT (-)**
3. **INPUT (+)**
4. **V-**

**6 OUTPUT**

**7 V+**

**8 COMP “B”**

**.046”**

**.068”**

**3 4**

**1 8 7**

**2**

**6**

**MASK**

**REF**

**1064**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004” Min.**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .046” X .068” DATE: 3/6/19**

**MFG: ADVANCED MICRO DEVICES THICKNESS .014” P/N: LM108A**

**DG 10.1.2**

#### Rev B, 7/19/02